FlexNoC® Interconnect IP

Arteris IP FlexNoC network-on-chip (NoC) interconnect IP improves performance, development time, power consumption and die size of system on chip (SoC) devices for consumer electronics, mobile, automotive and other applications.

Benefits

SILICON PROVEN

FlexNoC is the first commercial NoC interconnect and is shipping in over 1.5 Billion chips. It is the backbone SoC interconnect used by Samsung, Mobileye, Altera (Intel), Hisilicon (Huawei) and other industry leaders for their most important projects.

STATE-OF-THE-ART TECHNOLOGY

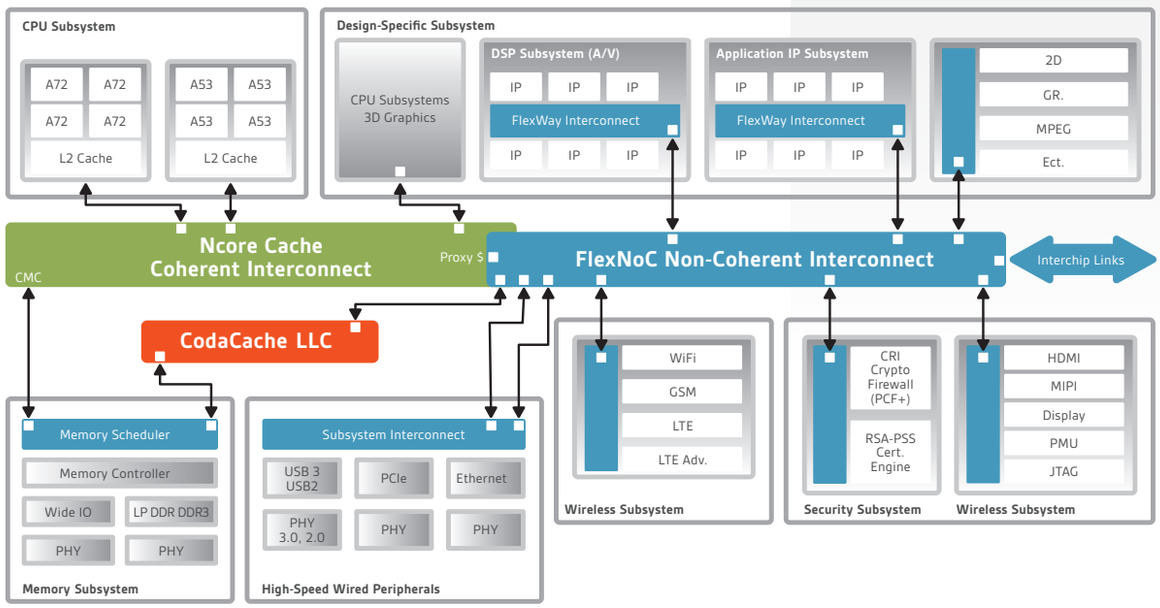
FlexNoC is continually updated with the latest technologies, including support for new protocols like AMBA® AHB5 and new capabilities like the FlexNoC Resilience Package for automotive ISO 26262 compliance and the PIANO Timing Assistance Package.

SCALABILITY & PRODUCTIVITY

Create SoCs using IP with any protocol (AMBA, OCP, PIF or proprietary) and scale up to 100s of IP blocks. Implement any topology (tree, ring, or mesh) while reducing development time through the use of automated simulation and verification technology.

Fast Facts

- Scales from 10s to 100s of IP blocks
- Protocol interoperability: AMBA AXI, AHB, APB; OCP; PIF; custom / proprietary
- Lowest die area & congestion
- Lowest latency & power
- Shortest design time
- Visual floorplan, area & timing closure estimation
- Integrated systemc simulation & UVM verification support
- Optimal QOS—bandwidth & latency
- Meet ISO 26262 ASIL D requirements



About Arteris IP

Arteris IP provides network-on-chip (NoC) interconnect IP to accelerate system-on-chip (SoC) semiconductor assembly for a wide range of applications from AI to automobiles, mobile phones, IoT, cameras, SSD controllers, and servers for customers such as Samsung, Huawei / HiSilicon, Mobileye, and Texas Instruments. Arteris IP products include the Ncore cache coherent and FlexNoC non-coherent interconnect IP, the CodaCache standalone last level cache, and optional Resilience Package (ISO 26262 functional safety) and PIANO automated timing closure capabilities. Customer results obtained by using the Arteris IP product line include lower power, higher performance, more efficient design reuse and faster SoC development, leading to lower development and production costs. For more information, visit www.arteris.com or find us on LinkedIn at https://www.linkedin.com/company/arteris.

Leading Industry Perspectives

"For years, Arteris technology has allowed us to continually increase the performance of each EyeQ ADAS SoC generation while reducing wire routing congestion and timing closure issues. The data protection technologies in the FlexNoC Resilience Package allow us to more easily implement state-of-the-art functional safety features in hardware, which simplifies the tasks of our software development teams as we strive to meet the most stringent ISO 26262 requirements."

ELCHANAN RUSHINEK
VICE PRESIDENT OF ENGINEERING
MOBILEYE

"Using Arteris FlexNoC allows us to reduce development time and manage project risk. FlexNoC's advanced quality-of-service and debugging features, combined with its multi-protocol support, allow Samsung SUHD TVs to reduce power consumption and die area for complex chips with more than 100 IP interfaces."

HAEJOO JEONG
VICE PRESIDENT, VISUAL DISPLAY BUSINESS
SAMSUNG ELECTRONICS

"In our never-ending efforts to improve efficiency, we've found Arteris technology is helping us meet our safety and time-to-market goals."

FABIO MARCHIO
VICE PRESIDENT, AUTOMOTIVE AND DISCRETE GROUP
STMICROELECTRONICS

"Using Arteris FlexNoC IP as the on-chip interconnect for our reference designs allows us to quickly customize each platform for our customers' performance, power, and ISO 26262 functional safety goals, while also providing a simple path to create follow-on derivative designs. This is particularly important to our automotive customers who want to quickly deploy and improve customized systems that accelerate their imaging, LIDAR point cloud, and 3D radar algorithms. Furthermore, our use of the FlexNoC Resilience Package helps ensure our customers can achieve the highest levels of ISO 26262 ASIL certification."

DR.-ING. JENS BENNDORF,
MANAGING DIRECTOR AND COO
DREAM CHIP TECHNOLOGIES

"Arteris FlexNoC interconnect IP allows us to create much more power-efficient designs while efficiently connecting novel hardware processing elements that accelerate artificial intelligence algorithms. Arteris interconnect IP is a key ingredient for creating the new state-of-the-art in power-efficient AI hardware."

MARK WU
VP OF TECHNOLOGY
CANAAN CREATIVE

"The Arteris network-on-chip technology scales much better, allowing us to increase the performance of our SoCs while reducing wire routing congestion and timing closure issues."

NOBUAKI OTSUKA
SENIOR MANAGER, MIXED SIGNAL IC DESIGN DEPARTMENT
TOSHIBA

ARTERIS IP

595 Millich Drive, Suite 200
Campbell, CA, 95008
arteris-support@arteris.com
+1 408 470 7300